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(54) Clock distribution control circuit for conserving power in computer systems.

(57) A NAPNOP circuit for decreasing energy consumption of all or a portion of a microprocessor based system which includes a delay circuit for inhibiting or slowing the output of the system clock pulses for a variable length of time equal to a multiple of N clock pulses where N is a positive integer. The NAPNOP circuit has an input element for inputting a STARTNAP signal which begins a nap period during which the system clock pulses ar inhibited or slowed, a clock input device for providing a plurality of selectable clock pulses as inputs to the delay circuit for controlling the operation of the computer system, and a gate element for terminating the nap period.

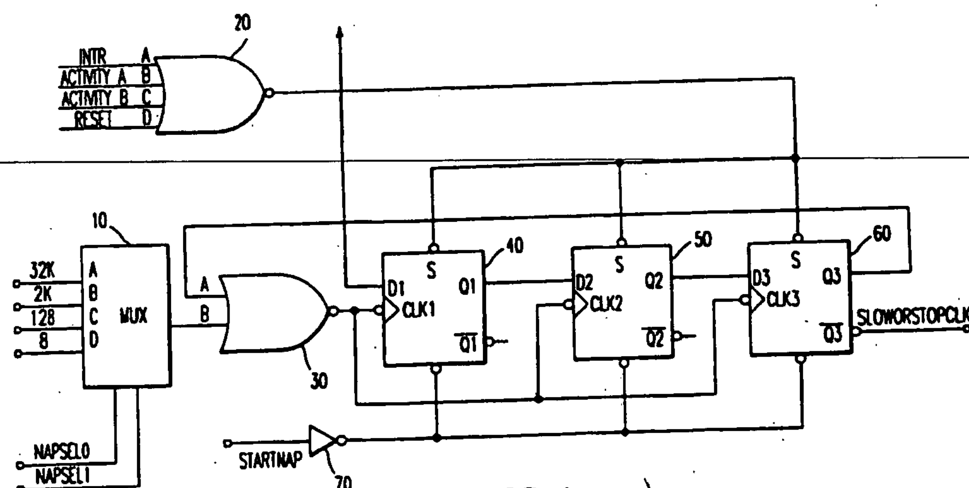

FIG. 1

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention r lates to the field of computing systems, and mor particularly, microproc ssor based systems, having improvements in n rgy conservation by decreasing the amount of lectricity used or extending the battery life of a battery operated system. The invention also serves to r duce heat generation by reducing wasted en rgy which can allow greater system reliability and reduced requirements for air flow, fans, or other cooling methods.

Discussion of the Related Art

In this invention, the NAP refers to a short wait period during which power savings are achieved by reducing the number of system circuit elements that are clocked or that are clocked at full speed, since clock frequency is proportional to power consumption.

The NOP function commonly used in computer systems today derives its name from a no-operation function. This instruction allows the execution of a no-operation state in order to create a short time delay. Most microprocessor based systems today provide some type of NOP function which only s rves to create a place holder in the processor instruction queue or to implement a fixed length short delay. In a typical microprocessor based system, the clock to the system remains fully active and the system power remains at peak l vels during a NOP function.

In prior art systems, computers or microproc ssor based systems have typically had to execute large numbers of NOPs or other types of dummy instructions to provide for delays of longer than one instruction cycle. One common problem with this type of methodology was that it suffered from large speed variations when the same programs were run on processors having different execution speeds.

In addition to a NOP function, another method commonly used to effect a wait period is to program a system timer or clock function to trigger an interrupt with an appropriate delay. However, this is substantially more complicated, requires additional system resources, and still requires that peak power be used needlessly.

Typically, power wasted in a system while in general use or during the xecution of an operation intended specifically to do nothing has not been an issue as little or no consideration has previously been given to the pow r c nsumption of th system. With the desire for extended battery life in battery operated microproc ss r bas d syst ms and energy conservation in AC electrically powered microprocessor based systems sponsored in part by environmental and economic concerns and the need to reduce heat generation in microprocessor based syst ms, the circuit according to the present inv ntion ov rcomes the for going drawbacks of the conventional systems.

SUMMARY OF THE INVENTION

Accordingly, one object of the present invention is to provide a novel circuit that creates and implements a NAPNOP function, which is used to slow or delay the output of the clock signal to the system, or a portion of the system, in order to thereby reduce overall power consumption and heat generation of the system. The NAPNOP would also create a wait period, much the same as a NOP has done historically, but with more flexibility and accuracy on duration. The NAPNOP can be triggered either by a software command or by hardware upon the detection of system condition, such as specific interrupts, software instructions, or code sequences. Each trigger produces a NAP period, that is, a wait period during which power savings are achieved by slowing or delaying the clock to all or a portion of the system.

This NAPNOP function can be used or triggered either in software or hardware form whenever it is determined that the system or some portion of the system is not involved in useful activity, in order to create power savings without sacrificing system performance.

A NAPNOP could also be used to slow the clock signal when the system is involved in useful activity thus saving power and reducing heat generation while degrading performance. Such use of the NAPNOP would be warranted when energy conservation was deemed more important than performance, for instance to prolong battery life when battery recharging would not be possible for an extended period. Or, such use of a NAPNOP might be warranted if the tradeoff between performance loss and energy or heat savings seemed reasonable. For instance, a 10% loss in performance might be tolerated to gain a ten fold increase in battery life.

The NAPNOP allows the reduction in system power consumption to extend battery life in battery operated microprocessor based systems or to reduce power consumption in AC powered microprocessor based systems, which can result in a savings in energy bills and reduce harmful effects f energy generation and dissipation on the environment.

Another effect of the NAPNOP function is to reduce heat generated by the microprocessor bas d system. As microprocessors and their en-

compassing systems contain increasing numbers of circuits and operate at high frequencies, heat generation becomes more problematic. By reducing wasted en rgy, heat generation is reduced. Sinc the ffects of heat can be harmful to system electronics, a reduction in heat generation can allow greater reliability. In addition, a reduction in heat can allow the removal of cooling devices such as fans and heat sinks, or a reduction or elimination of requirements for cooling air or liquid flow or the elimination of thermal measuring devices used to provide feedback on extreme heat conditions.

In order to achieve the above and other objects, the present invention includes a NAPNOP circuit for inhibiting or slowing the output of system clock pulses. This circuit includes a delay circuit for preventing the output of the system clock pulses for a variable length of time equal to a multiple of N clock pulses where N is a positive integer. The NAPNOP circuit has an input element for inputting a STARTNAP signal which begins a nap period during which the system clock pulses are prevented from being output from the delay circuit. The NAPNOP circuit also includes a clock input device for providing a plurality of clock pulses as inputs to the delay circuit for controlling the operation of the computer system, and a gate element for terminating the nap period and permitting the clock pulses to be output to the computer system.

In a preferred embodiment, the NAPNOP circuit includes a plurality of series connected flip flops, each of which delays the output of the clock signal by one clock pulse. Therefore, the period of time for delaying the output of the clock signal to the computer system can be set to any desired value based on the number of series connected flip flops employed. A STARTNAP signal is used to trigger the onset of the delay period during which the output of the final flip flop of the series connection is inhibited. An additional gate element is provided for immediately ending the nap period if, for example, during a nap an interrupt or other activity input command is generated. As an example, a keyboard input could generate such an interrupt.

The NAPNOP function according to the invention provides savings in power during nap periods. It also permits a more exact timing of delay periods and allows for more flexibility in the triggering or ending of delay periods. The NAPNOP is also effective in reducing power consumption and extending battery life in battery operated computer systems. It is further effective in reducing power consumption in AC powered computer systems so as to reduce the energy consumed by desktop systems. In both battery and AC powered systems, the heat generation of the syst m would also be reduced as a consequence of th reduction in power consumed. This provides for greater system reliability, and a reduction in the amount of cooling needed. This allows for more compact computer enclosures as the amount of air flow f r cooling purposes is not as critical. Also, the NAPNOP circuit according to the invention may but need not diminish th system performance in order to achieve its power savings.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

Figure 1 represents a specific embodiment of the NAPNOP circuit according to the present invention; and

Figure 2 illustrates a timing sequence for the triggering of the high/low states of the various elements of the NAPNOP circuit shown in Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, and more particularly to Figure 1 thereof, there is shown one embodiment of the NAPNOP circuit according to the present invention. The NAPNOP circuit shown in Figure 1 provides a method of implementing a short time delay function while at the same time saving power. The NAPNOP circuit according to the invention operates by providing several real time delay options which can be triggered by software instructions, for example. These delay options could typically be anywhere from nanoseconds to hundreds of milliseconds. Further, this circuit could be implemented either internally within the processor itself or externally within some type of system controller. The nap period could be triggered by a system activity that indicated no useful activity was being performed or indicated that a loss in performance was reasonably warranted. Additionally, the nap period could be triggered by a software NAPNOP command. The NAPNOP could be implemented to create a fixed time delay or could be implemented to allow a user time delay or could be implemented to allow a user selectable time delay. In the latter case as in this embodiment, a command to select the tim delay would precede the NAPNOP command. Or, th circuit could be implemented to allow system conditions to select the appropriate wait period in a programmable configuration. During this wait period, the system clock could be stopped within the microprocessor at th

phase lock loop output of the clock or the microprocessor's clock could be stopped externally.

During a triggered delay, the system clock would be stopped within the microprocessor at a phase lock loop (PLL) output of the clock. Similarly, other system clocks, other d vices, or oth r partitions of the system circuitry could be powered down during this delay in order to save additional pow r. A feature of the NAPNOP circuit is its ability t exit or terminate the delay period immediately upon any type of system interrupt or activity. Examples of system interrupts or activities that could terminate the NAPNOP include standard system int rrupts as well as any special purpose interrupts such as system management interrupt (SMI) or a non-maskable interrupt (NMI). This ensures that ther is no delay in responding to any significant syst m activity. For different situations it is useful to pr vide several options. The NAPNOP circuit of the invention could, for instance, exit on interrupt, not xit until done, or exit during interrupt or resum after interrupt if not already beyond its allotted time.

An example of an application of the NAPNOP circuit according to the present invention would be for use in a user interface program. For example, a program may write information to a video screen and th n be required to wait some period of time while the user reads the screen or waits for an input from the keyboard or other interface device, before proceeding to write further information. Similarly, there are many other situations that require programs to wait for various periods of time.

Another example is during a hard disk read. The program must first request data from the disk and then wait for the disk controller to locate the appropriate data and respond, which might take several milliseconds. During this time period, it is d sirable to prevent the output of the system clock to the various elements of the computer system in order to conserve system power. The NAPNOP function can be used very conveniently for this type of delay function. Because it is capable of programmable delays that can be much longer than a standard NOP and since multiple NAPNOPs can be strung together, any desired delay time period can be created. A NAPNOP circuit is more convenient and flexible in providing timing delays than conventional NOP loops. A conventional NOP loop would have multiple dummy instructions where the only purpose is to kill time.

The NAPNOP circuit shown in Figure 1 includes a multiplexer 10 having a plurality of inputs provided with clocks of differ nt fr quencies. For example, a two bit NAPSEL signal is used to select anyone of four clock frequ nci s, which are used to establish the delay period of the NAPNOP. NAPSEL0 and NAPSEL1 would typically be driven from outputs of programmable register bits. NAPSEL0 and NAPSEL1 are gated into a multiplexer which could select, for example, 8, 128, 2000 or 32,000 Hertz clock signals. The selected clock then serves as a B input to OR gate 30. If the A input is l w or "0" then the B signal, or equivalently, the clocking signal, is passed as the input to the series of three flip flops 40, 50 and 60. It should be noted that the inverter on the output of the OR gate 30 and the inverter on each of the clock inputs to the three flip flops will cancel each other. On the other hand, if the A signal is high or "1" then a constant "1" is passed as the input to each of the three flip flops and the clocking is essentially stopped. The data input to the flip flop 40 is always pulled high or "1". The output of flip flop 40 and flip flop 50 are used as the inputs to flip flop 50 and flip flop 60, respectively. The output of flip flop 60 then serves as the A input to OR gate 30. In this implementation, any one of four input signals may serve to set all three flip flops. The four signals in this case are INTR (an interrupt), ACTIVITYA, ACTIVITYB, or a RESET signal. ACTIVITYA and ACTIVITYB could be any activity in the system derived from a set of complex functions or from an input condition. All four conditions are gated through OR gate 30 and any one of the signals being active or high would cause this set condition to be met. It should be noted that the inverter on the output of the OR gate 20 and the inverter on the "S" terminal or set input to the flip flops serve to cancel each other out.

A STARTNAP signal is used to reset the three flip flops 40, 50 and 60. The STARTNAP signal could begin a nap period in response to a software NAPNOP command, a string of software commands suitable for replacement with a NAPNOP, or in response to a system activity including detection of lack of useful system activity. Any number of system activities could be used to trigger a nap period depending on the system application, implementation, or conditions. The STARTNAP signal, therefore, begins the nap period because the output of the flip flop 60, or Q3, is equal to the input of OR gate 30, i.e., signal A. With signal A pulled low by the reset action of STARTNAP, the clocking of input B is the clock input to flip flop 40. The STARTNAP signal is inverted by inverter element 70 which serves to cancel the inverter on the reset terminal of the flip flops. The SLOWORSTOPCLK signal is the inverse of Q3 (or signal A) and goes high with the high state of the STARTNAP signal. The input to flip flop 40 is always pulled high and therefore, presuming that a clock signal has been selected by the multiplex r 10, the output of flip flop 40, Q1, goes high at the first rising edge of the clock input B. The input to flip flop 50, D2, quals Q1. With the input to flip flop

50, D2, now high, the output, Q2, goes high on the next rising edg of the clock signal input B. This output, Q2, is qual to the input of flip flop 60, D3. With the input of flip flop 60, D3, now high, the output Q3 is pulled high at the next rising edge of th clock. The SLOWORSTOPCLK signal is the inverse of Q3; it is pulled low thus ending the nap. Without an interrupt or activity triggering the set condition from OR gate 20, the nap is a multiple of three clock periods. It should be noted, however, that the nap period could be set to be any desirable number of clock pulses simply by adding or deleting one or more of the series-connected flip flops. If any of the four set conditions input to OR gate 20, i.e., the INTR, ACTIVITYA, ACTIVITYB, or RESET are active, the flip flop outputs, Q1, Q2 and Q3 would all be pulled high. This sets the signal A to a "1" or a high state and stops the clocking action by blocking signal B. With Q3 high, the SLOWORSTOPCLK signal is low, thus not allowing a nap. Thus, the nap can be prevented or ended immediately by virtue of some interrupt or activity signal.

By using the multiplexer 10 to select one of the plurality of different clock pulse frequencies, the present invention allows for further variations in the length of the nap periods by selecting a different input frequency clock pulse. As such, the present invention provides two ways of delaying the output of a clock signal, i.e., by adding more cascade-connected flip flips or by choosing a clock pulse signal having a lower frequency. Also, the length of the nap can be changed at any time by the action of one or more different activities or other interrupt signals which would immediately end the nap.

The timing sequence shown in Figure 2 will now be described with respect to the inputs and outputs of the various elements of Figure 1. As shown, a clock signal B is selected from the multiplexer 10 by the input signals NAPSEL0 and NAPSEL1. This clocking signal B will be output to the inputs of each of the flip flops 40, 50, 60, the output Q3 of flip flop 60 will be "1" and therefore, the input signal A will also be "1". As can be seen from Figure 2, when the STARTNAP signal goes high, the output of flip flop 40, Q1, will go low because the STARTNAP signal will reset flip flop 60 so that the output Q3 is zero and the SLOWORSTOPCLK signal goes high, thus starting the nap. As can also be seen from Figure 2, the outputs Q2 and Q3 of flip flops 50 and 60, respectively, will also go low at the beginning of the nap, i.e., the point at which STARTNAP goes high. However, upon the b ginning of the next clock cycle, the output Q1 will again go high, but the outputs Q2 and Q3 of the next two flip flops will have to wait one and two additional clock pulses, respectively, before they go back high. At the point when the third flip flop 60 finally goes high again, the SLOWORSTOPCLK signal will then return to the low state and the clock will again be output to the computer system. Therefore, the delay period, i.e., the nap period, will be equal to a value of thr e successive clock pulses, corresponding to the three successive flip flops 40, 50 and 60. However, a number of additional flip flops could be similarly connected in order to further extend this delay period, or fewer flip flops could be used in order to reduce the delay period. Also, by selecting one of a plurality of different clock frequencies, the delay period could be further varied.

It should also be noted that if an activity of appropriate type occurred such as to drive signal Y1 low, at any point during the nap period, this would immediately terminate the nap by forcing signal "SLOWORSTOPCLK" back low while simultaneously forcing all flipflops back to their idle state which is with their Q outputs high.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise then as specifically described herein.

Claims

1. A circuit for inhibiting clock pulses from being output to a microprocessor based system, comprising:

   means for accepting a software controlled signal indicative of an amount of time for which said clock pulses are to be inhibited from being output to said microprocessor based system;

   means for inhibiting said clock pulses for said amount of time; and

   means for providing a shutdown signal for the powering down of at least a portion of said microprocessor based system.

2. A circuit for slowing or inhibiting the output of clock pulses to a microprocessor based system for a specific period of time, initiated by a specific trigger condition, comprising:

   a delay circuit for preventing the output of said system clock pulses for a variable length of time equal to a multiple of N clock pulses where N is a predetermined positive integer;

   means, coupled to said delay circuit, for inputting a first signal which begins a nap period during which said system clock pulses are prev nted from being output from said delay circuit to said microprocessor based system;

   clock input means, coupled to said d lay

circuit, for providing a clock pulse signal as an input to said delay circuit which functions to control the operati n of said microprocessor based system; and

gat means, coupled to said delay circuit, for applying a second signal to said d lay circuit in order to thereby terminate said nap period by permitting said clock pulse signal to be output from said delay circuit to said microprocessor based system.

3. Th circuit according to Claim 2, wherein said clock input means comprises:

means for selecting one of a plurality of different frequency clock pulse signals, each of which includes a plurality of synchronous clock pulses.

4. The circuit according to Claim 3, wherein said means for selecting one of said plurality of different frequency clock pulse signals comprises:

a multiplexer.

5. The circuit according to Claim 4, wherein said multiplexer includes a plurality of first inputs for receiving said plurality of clock pulse signals and at least one second input for determining the frequency of the clock pulse signal which will be output to said delay circuit.

6. The circuit according to Claim 3, wherein said delay circuit comprises:

a plurality of series-connected flip flop elements.

7. The circuit according to Claim 6, wherein said plurality of flip flop elements equals N in number.

8. The circuit according to Claim 7, wherein the output of the nth flip flop element is applied as an input to said delay circuit in order to control the input of said selected clock pulse signal to the first flip flop element of said N series-connected flip flop elements.

9. The circuit according to Claim 8, further comprising:

a gate circuit which receives, as a first input, the selected clock pulse signal, and as a second input, the output of said nth flip flop element.

10. The circuit according to Claim 9, wh rein said selected clock pulse signal is output from th delay circuit wh n the output of said nth flip flop lement goes high.

11. A method for delaying a clock pulse signal from being output to a microprocessor based system, comprising the steps of:

providing a clock pulse signal of a predetermined fr qu ncy as an input to a delay circuit;

inhibiting said clock pulse signal from being output to said microprocessor based system for a variable length of time equal to a multiple of N clock pulses where N is a predetermined positive integer; and

terminating said step of inhibiting said clock pulse signal from being output to said microprocessor based system upon the application of an external signal to said delay circuit.

12. The method according to Claim 11, wherein said step of providing said clock pulse signal of predetermined frequency as an input to said delay circuit comprises:

selecting one of a plurality of different frequency clock pulse signals for input to said delay circuit.

13. The method according to Claim 12, wherein said step of providing said clock pulse signal of predetermined frequency as an input to said delay circuit further comprises:

inputting a plurality of different frequency clock pulse signals to a multiplexer which receives at least one additional input signal for determining the clock pulse signal to be input to said delay circuit.

14. The method according to Claim 11, wherein said step of inhibiting said clock pulse signal from being output to said microprocessor based system comprises the step of:

inputting a second external signal to a first circuit element of said delay circuit which prevents the clock pulse signal from being output to said microprocessor based system.

15. The method according to Claim 11, wherein said step of inhibiting said clock pulse signal from being output to said microprocessor based system further comprises the step of:

maintaining an output signal of said delay circuit in a state which prevents the output of clock pulses to said microprocessor based system.

16. The method according to Claim 15, wherein said step of maintaining said output signal of said d lay circuit in a state which pr vents the output of clock pulses to said microprocessor based syst m comprises the steps of:

maintaining the output of the nth flip flop element of N flip flop elements included in said delay circuit in a state which prevents said clock puls s from being output to said microprocessor bas d system.

17. The method according to Claim 16, further comprising the step of:
applying a first high signal to the input of a first flip flop element of said delay circuit during a first clock pulse of said clock pulse signal, applying a second high signal to the input of a second flip flop element of said delay circuit during a second clock pulse of said clock pulse signal and applying a third high signal to the input of a third flip flop element of said delay circuit, thereby causing said clock pulse signal to be output from said delay circuit to the microprocessor based system.

18. A circuit for delaying a clock pulse signal from being output to a microprocessor based system, comprising:
clock input means for providing one of a plurality of clock pulse signals having different frequencies to an input terminal;
means, coupled to said clock input means, for selecting one of said plurality of clock pulse signals on the basis of predetermined information concerning the length of the delay of the output of the clock pulse signal to the microprocessor based system; and
output means, coupled to said clock input, means for outputting said selected one of said plurality of clock pulse signals to said microprocessor based system.

19. The circuit according to Claim 18, wherein said clock input means comprises a multiplexer.

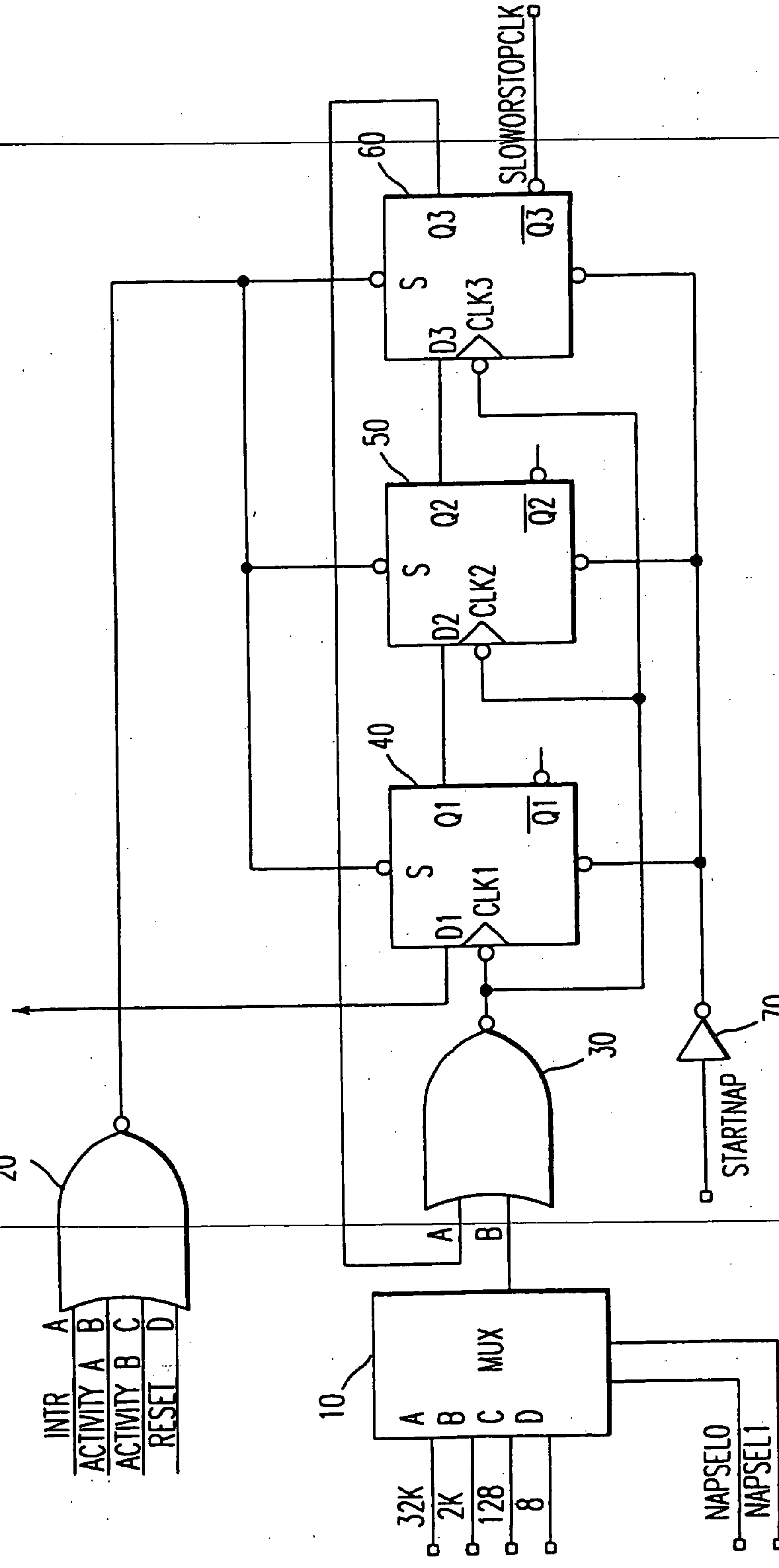
20. The circuit according to Claim 18, wherein said means for selecting one of said plurality of clock pulse signals comprises at least one external signal which is input to said clock input means.

21. The circuit according to Claim 18, wherein said output means comprises at least one flip flop element.

22. A method for delaying a clock pulse signal from being output to a microprocessor based system, comprising the steps of:
providing one of a plurality of clock pulse signals having different fr quencies to an input terminal;
selecting one of said plurality of clock pulse signals on the basis of predetermined information concerning the length of the delay of the output of the clock pulse signal to the microprocessor based system; and
outputting said selected one of said plurality of clock pulse signals to said microproc ssor based system.

23. The method according to Claim 22, wherein said step of selecting one of said plurality of clock pulse signals comprises the step of:
inputting an external signal to a multiplexer.

24. The method according to Claim 22, wherein said step of outputting said selected one of said plurality of clock pulse signals comprises the step of:
outputting said selected clock pulse signal from a flip flop element to said microprocessor based system.


SLOWORSTOPCLK
60
Q3
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D3
CLK3
50
Q2
$\overline{Q2}$
S
D2
CLK2
40
Q1
$\overline{Q1}$
S
D1
CLK1
20
30
70
STARTNAP
A
B
INTR
ACTIVITY A
ACTIVITY B
RESET
A
B
C
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10
MUX
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NAPSEL0
NAPSEL1

FIG. 1

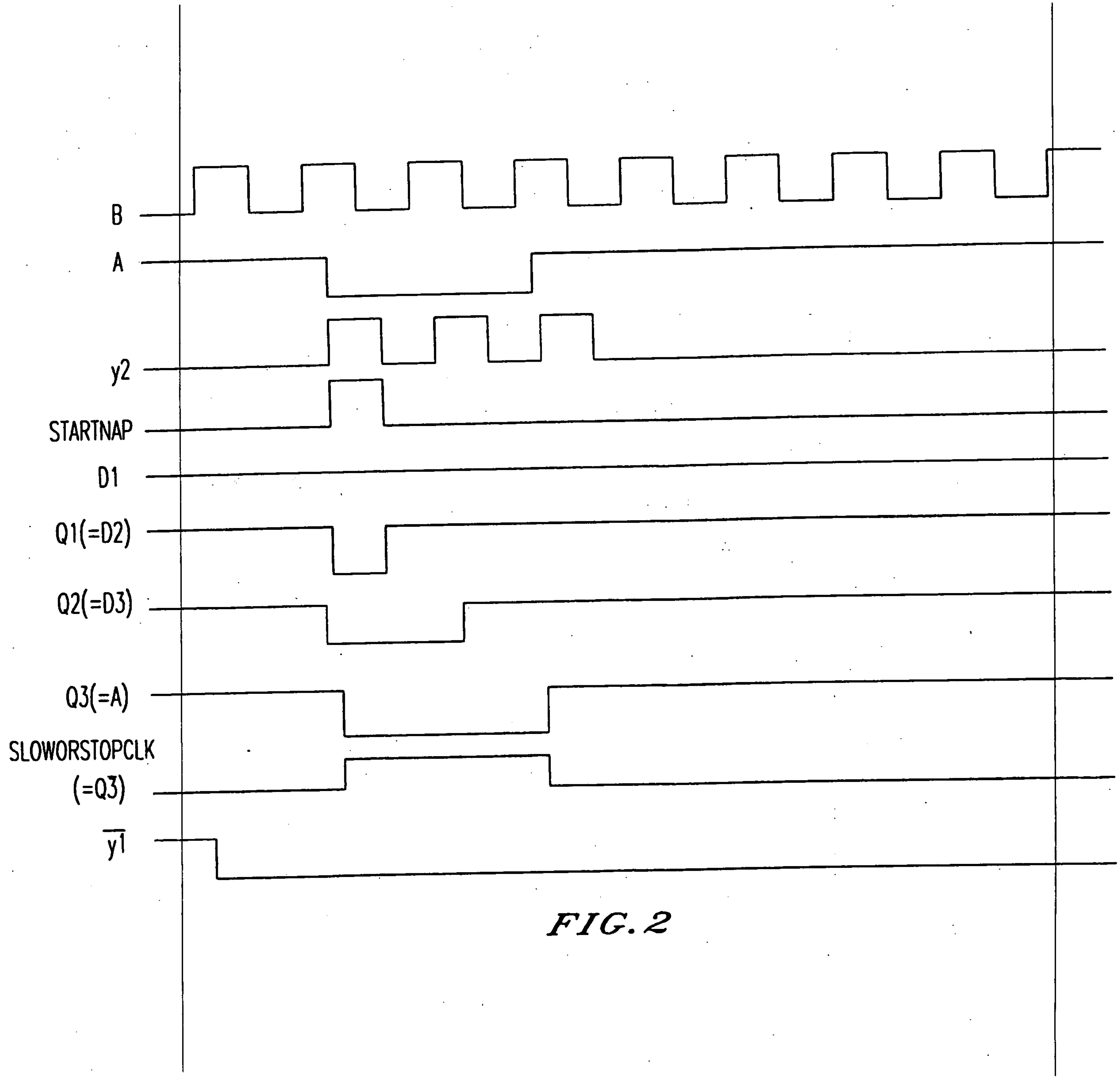

B
A
y2
STARTNAP
D1
Q1(=D2)
Q2(=D3)
Q3(=A)
SLOWORSTOPCLK
(=Q3)
$\overline{y1}$

FIG. 2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 40 2884

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	EP-A-0 501 655 (IBM CORP.) * column 1, line 55 - column 2, line 9-13 * * column 3, line 9 - line 13 * * figure 2 * ---	1,2,11 18,22	G06F1/32
A	GB-A-2 246 455 (PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED) * abstract; figure 1 * ---	3	
A	WO-A-93 20498 (SEIKO EPSON CORP.) * abstract * -----	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 March 1995	Ciarelli, N

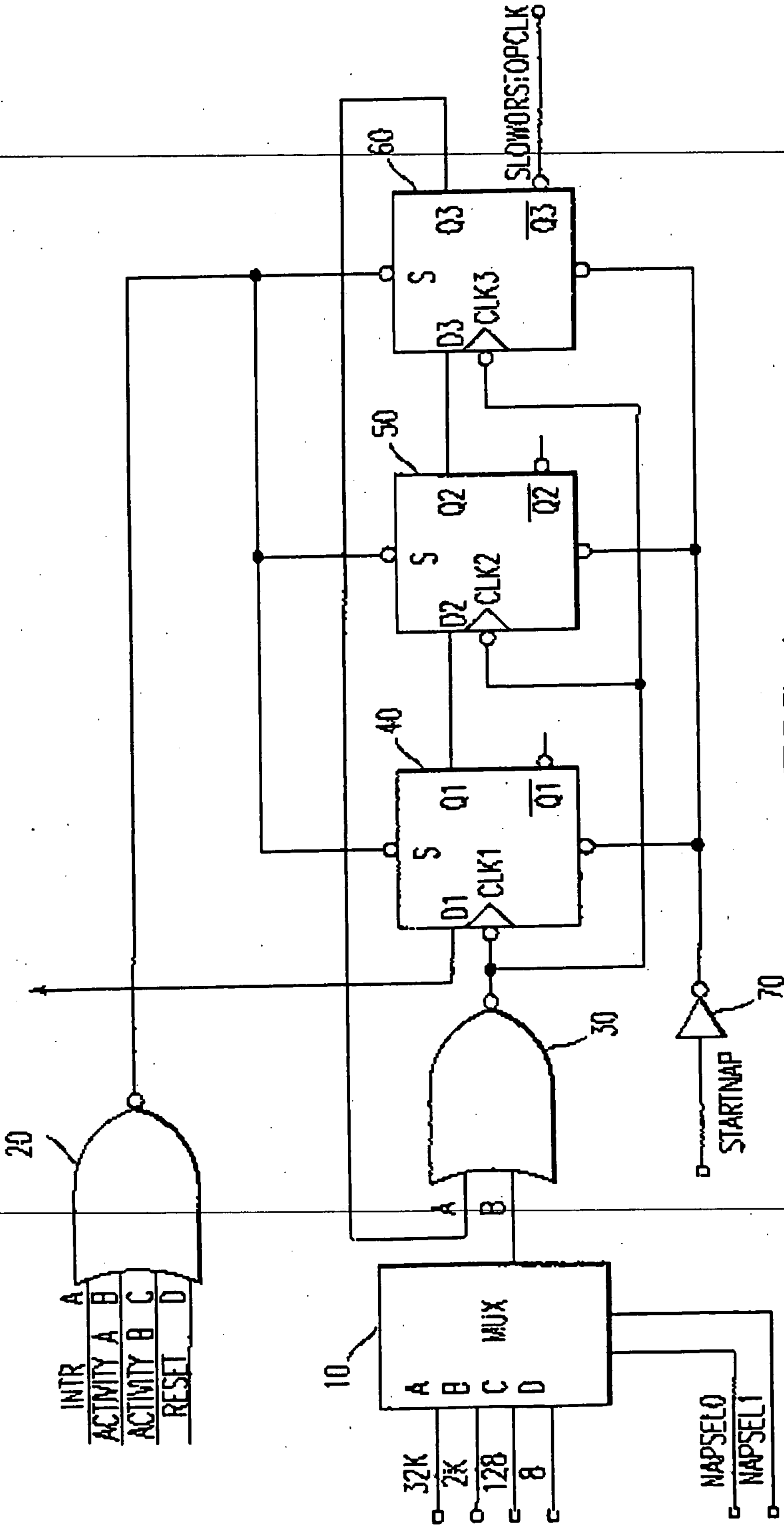
CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)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Q3
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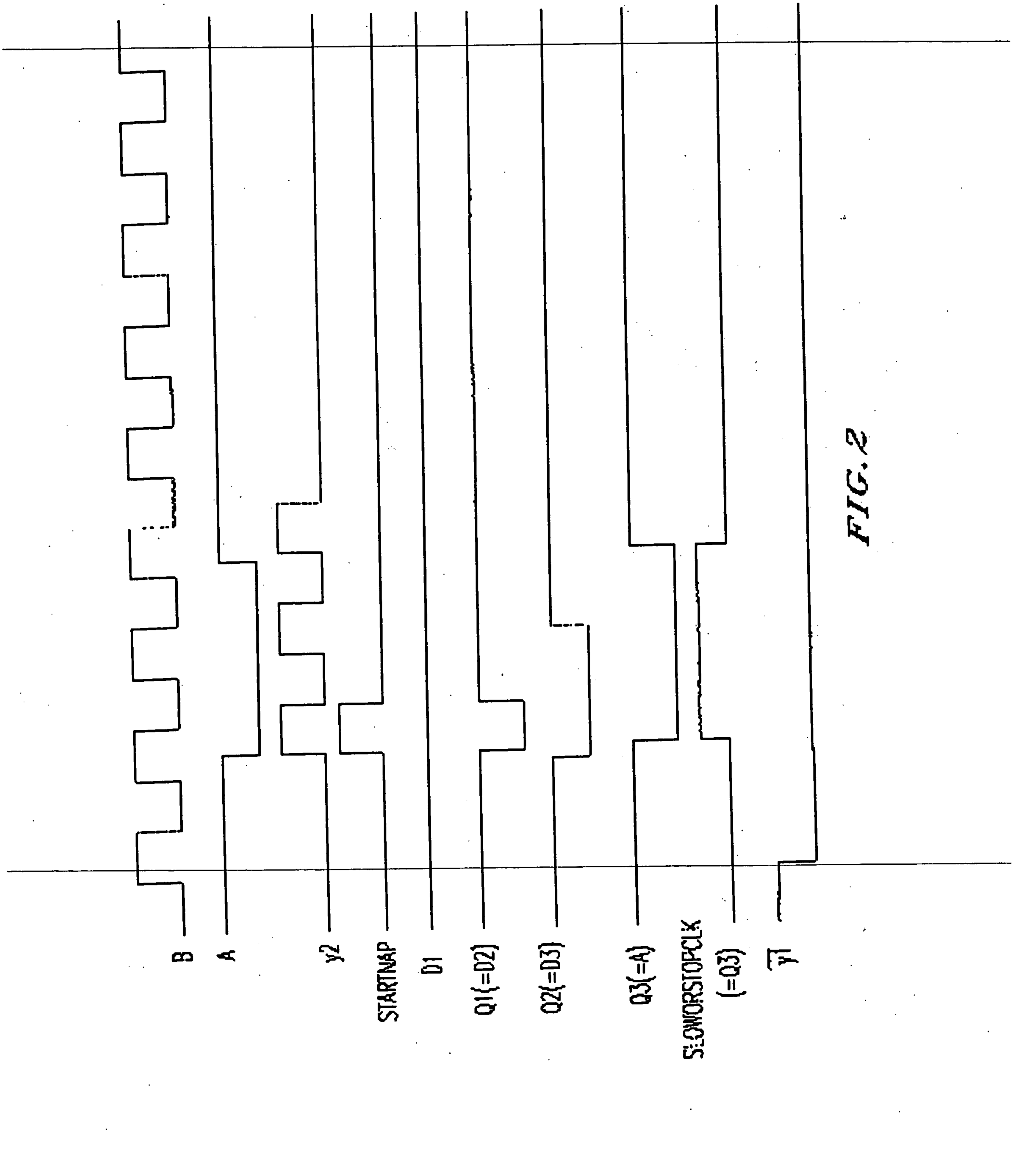
D3
CLK3
50
Q2
$\overline{Q2}$
S
D2
CLK2
40
Q1
$\overline{Q1}$
S
D1
CLK1
20
30
70
STARTNAP
A
B
INTR
ACTIVITY A
ACTIVITY B
RESET
A
B
C
D
10
MUX
A
B
C
D
32K
2K
128
8
NAPSEL0
NAPSEL1

FIG. 1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A
y2
STARTNAP
D1
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Q2(=D3)
Q3(=A)
SLOWORSTOPCLK
(=Q3)
$\overline{y1}$

FIG. 2